Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**EMITTER**

**BASE**

**.041”**

**.041”**

**CHIP BACK IS COLLECTOR**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: E = .008” X .008” B = .007**

**Backside Potential: COLLECTOR**

**Mask Ref: G12**

**APPROVED BY: DK DIE SIZE .041” X .041” DATE: 10/19/21**

**MFG: ZETEX THICKNESS .007” P/N: ZTX750**

**DG 10.1.2**

#### Rev B, 7/19/02